What is claimed is:

1. A precompensation circuit for magnetic recording of data signals comprising:

a clock to generate clock signals at a predetermined rate in successive clock periods to clock the data signals to be recorded;

a clock delay generator to generate clock delay data relative to the generated clock signal for each successive data signal to be recorded responsive to a pattern of adjacent data signals; and

$n > 1$ clock delay units to control recording times of the successive data signals, each clock delay unit operating to generate an output signal for determining the recording time of one data signal in each sequence of n successive data signals responsive to the clock delay data received by the clock data unit for the one data signal in the sequence.

2. A precompensation circuit for magnetic recording of data signals according to Claim 1, wherein a clock delay unit receives the clock delay data corresponding to an mth data signal of the successive data signals in a clock period during which the clock delay unit that received the clock delay data corresponding to the (m-n+1)th data signal of the successive data signals generates the output signal for determining the recording time of the (m-n+1)th data signal.

3. A precompensation circuit for magnetic recording of data signals according to Claim 1, wherein each clock delay unit comprises a reprogrammable clock delay unit that is reprogrammed for the one data signal received in each sequence of n successive data signals.

4. A precompensation circuit for magnetic recording of data signals according to Claim 1, wherein each pattern of adjacent data signals includes at least one of a pattern of data signals immediately preceding the data signal for which the clock delay data is generated and a set of data signals immediately succeeding the data signal for which the clock delay data is generated.

5. A precompensation circuit for magnetic recording of data signals according to Claim 1, wherein each pattern of adjacent data signals includes a pattern of data signals surrounding the data signal for which the clock delay data is generated.

6. A precompensation circuit for magnetic recording of data signals according to Claim 1, further comprising a selector to select the output signals of the n clock delay units successively in each n data signal sequence to control the recording times of the successive data signals of the sequence so that the clock delay data for the mth data signal is received by one of the n clock delay units while the output signal of the clock delay unit that is to receive the m+1th data signal controls the recording time of the (m-n+1)th data signal.

7. A precompensation circuit for magnetic recording of data signals according to Claim 1, wherein the clock delay generator comprises a look up table responsive to the pattern of adjacent data signals for forming clock delay data relative to the generated clock signal for each successive data signal.

8. A precompensation circuit for magnetic recording of data signals according to Claim 1, further comprising a reference clock delay unit responsive to the generated clock signals for producing reference clock delay information corresponding to the predetermined clock rate.

9. A precompensation circuit for magnetic recording of data signals according to Claim 8, wherein the clock delay generator comprises:

a look up table responsive to the pattern of adjacent data signals for each data signal to form clock delay information; and

a combining unit to combine the produced reference clock delay information with the look up table formed clock delay information to generate the clock delay data for the data signal.

10. A precompensation circuit for magnetic recording of data signals according to Claim 8, wherein the reference clock delay unit comprises a

reprogrammable reference clock delay unit which is reprogrammed responsive to a change in the predetermined clock rate.

11. A precompensation circuit for magnetic recording of data signals according to Claim 9, further comprising a calibrator responsive to a change in the predetermined clock rate for calibrating each of the n clock delay units to the changed predetermined clock rate.

12. A precompensation circuit for magnetic recording of data signals according to Claim 11, wherein the calibrator includes a comparator for comparing the output signal of the reference clock delay unit to the output signals of the n clock delay units to form an offset value for each of the n clock delay units.

13. A precompensation circuit for magnetic recording of data signals according to Claim 1, wherein each clock delay unit includes an interpolator for interpolating the received clock delay data.

14. A method of precompensating magnetic recording of data signals comprising the steps of:

generating clock signals at a predetermined rate in successive clock periods to clock the data signals to be recorded;

generating clock delay data relative to the generated clock signal for each successive data signal to be recorded responsive to a pattern of adjacent data signals; and

sequentially controlling recording times of the successive data signals by n>1 clock delay units, each clock delay unit generating an output signal for determining the recording time of one data signal in each sequence of n successive data signals responsive to the clock delay data received by the clock data unit for the one data signal of the sequence.

15. A method of precompensating magnetic recording of data signals according to Claim 14, wherein a clock delay unit receives the clock delay data corresponding to an mth data signal of the successive data signals in a clock period during which the clock delay unit that received the clock delay data corresponding to the (m-n+1)th data signal of the successive data signals generates the output signal for determining the recording time of the (m-n+1)th data signal.

16. A method of precompensating magnetic recording of data signals according to Claim 14, wherein each clock delay unit is reprogrammed for the one data signal received in each sequence of n successive data signals.

17. A method of precompensating magnetic recording of data signals according to Claim 14, wherein each pattern of adjacent data signals includes at

least one of a pattern of data signals immediately preceding the data signal for which the clock delay data is generated and a set of data signals immediately succeeding the data signal for which the clock delay data is generated.

18. A method of precompensating magnetic recording of data signals according to Claim 14, wherein each pattern of adjacent data signals includes a pattern of data signals surrounding the data signal for which the clock delay data is generated.

19. A method of precompensating magnetic recording of data signals according to Claim 14, further comprising selecting the output signals of the n clock delay units successively in each n data signal sequence to control the recording times of the successive data signals of the sequence so that the clock delay data for the mth data signal is received by one of the n clock delay units while the output signal of the clock delay unit that is to receive the m+1th data signal controls the recording time of the (m-n+1)th data signal.

20. A method of precompensating magnetic recording of data signals according to Claim 14, wherein the generating of the clock delay data includes obtaining clock delay information from a look up table responsive to the pattern of adjacent data signals for forming clock delay data relative to the generated clock signal for each successive data signal.

21. A method of precompensating magnetic recording of data signals according to Claim 14, further comprising producing reference clock delay information corresponding to the predetermined clock rate responsive to the generated clock signals.

22. A method of precompensating magnetic recording of data signals according to Claim 21, wherein the generation of the clock delay data includes:

obtaining clock delay information from a look up table responsive to the pattern of adjacent data signals for each data signal; and

combining the produced reference clock delay information with the look up table formed clock delay information to generate the clock delay data for the data signal.

23. A method of precompensating magnetic recording of data signals according to Claim 21, wherein the reference clock delay unit is reprogrammed responsive to a change in the predetermined clock rate.

24. A method of precompensating magnetic recording of data signals according to Claim 22, further comprising calibrating each of the n clock delay units to the changed predetermined clock rate responsive to a change in the predetermined clock rate.

25. A method of precompensating magnetic recording of data signals according to Claim 24, wherein the calibration includes comparing the output signal of the reference clock delay unit to the output signals of the n clock delay units to form an offset value for each of the n clock delay units.

26. A method of precompensating magnetic recording of data signals according to Claim 14, wherein each clock delay unit interpolates the received clock delay data.

27. A precompensation circuit for magnetic recording of data signals comprising:

clock means for generating clock signals at a predetermined rate in successive clock periods to clock the data signals to be recorded;

clock delay generating means for generating clock delay data relative to the generated clock signal for each successive data signal to be recorded responsive to a pattern of adjacent data signals; and

$n > 1$ clock delay means for controlling recording times of the successive data signals, each clock delay means operating to generate an output signal for determining the recording time of one data signal in each sequence of n successive data signals responsive to the clock delay data received by the clock data means in the sequence for the one data signal.

28. A precompensation circuit for magnetic recording of data signals according to Claim 27, wherein a clock delay means receives the clock delay data corresponding to an mth data signal of the successive data signals in a clock period during which the clock delay means that received the clock delay data corresponding to the (m-n+1)th data signal of the successive data signals generates the output signal for determining the recording time of the (m-n+1)th data signal.

29. A precompensation circuit for magnetic recording of data signals according to Claim 27, wherein each clock delay means comprises reprogrammable clock delay means that is reprogrammed for the one data signal received in each sequence of n successive data signals.

30. A precompensation circuit for magnetic recording of data signals according to Claim 27, wherein each pattern of adjacent data signals includes at least one of a pattern of data signals immediately preceding the data signal for which the clock delay data is generated and a set of data signals immediately succeeding the data signal for which the clock delay data is generated.

31. A precompensation circuit for magnetic recording of data signals according to Claim 27, wherein each pattern of adjacent data signals includes a

pattern of data signals surrounding the data signal for which the clock delay data is generated.

32. A precompensation circuit for magnetic recording of data signals according to Claim 27, further comprising a selecting means for selecting the output signals of the n clock delay means successively in each n data signal sequence to control the recording times of the successive data signals of the sequence so that the clock delay data for the mth data signal is received by one of the n clock delay means while the output signal of the clock delay means that is to receive the m+1th data signal controls the recording time of the $(m \cdot n+1)$th data signal.

33. A precompensation circuit for magnetic recording of data signals according to Claim 27, wherein the clock delay generating means comprises means responsive to the pattern of adjacent data signals for looking up clock delay data relative to the generated clock signal for each successive data signal.

34. A precompensation circuit for magnetic recording of data signals according to Claim 27, further comprising a reference clock delay means responsive to the generated clock signals for producing reference clock delay information corresponding to the predetermined clock rate.

35. A precompensation circuit for magnetic recording of data signals according to Claim 34, wherein the clock delay generating means comprises:

look up means responsive to the pattern of adjacent data signals for each data signal for forming clock delay information; and

combining means for combining the produced reference clock delay information with the look up means formed clock delay information to generate the clock delay data for the data signal.

36. A precompensation circuit for magnetic recording of data signals according to Claim 34, wherein the reference clock delay means comprises a reprogrammable reference clock delay means which is reprogrammed responsive to a change in the predetermined clock rate.

37. A precompensation circuit for magnetic recording of data signals according to Claim 35, further comprising a calibration means responsive to a change in the predetermined clock rate for calibrating each of the n clock delay units to the changed predetermined clock rate.

38. A precompensation circuit for magnetic recording of data signals according to Claim 37, wherein the calibration means includes a comparing means for comparing the output signal of the reference clock delay means to the output signals of the n clock delay means to form an offset value for each of the n clock delay means.

39. A precompensation circuit for magnetic recording of data signals according to Claim 27, wherein each clock delay means includes interpolating means for interpolating the received clock delay data.

40. In a precompensation circuit for magnetic recording of data signals having a clock generating clock signals at a predetermined rate in successive clock periods to clock the data signals to be recorded, a computer usable medium having computer readable program units embodied therein comprising:

a first program unit for determining clock delay data for each successive data signal responsive to a pattern of adjacent data signals; and

a second program unit for controlling sequential operation of $n > 1$ programmable clock delay units to determine the recording time of the successive data signals,

wherein each programmable clock delay unit is controlled to generate an output signal for determining the recording time of one of the data signals in each sequence of n successive data signals responsive to the clock delay data received by the clock data unit for the one data signal in the sequence.

41. In a precompensation circuit for magnetic recording of data signals having a clock generating clock signals at a predetermined rate in successive clock periods to clock the data signals to be recorded, a computer usable medium

having computer readable program units embodied therein according to Claim 40, wherein the second program unit controls a clock delay unit to receive the clock delay data corresponding to an mth data signal of the successive data signals in a clock period during which the clock delay unit that received the clock delay data corresponding to the (m·n+1)th data signal of the successive data signals generates the output signal for determining the recording time of the (m·n+1)th data signal.

42. In a precompensation circuit for magnetic recording of data signals having a clock generating clock signals at a predetermined rate in successive clock periods to clock the data signals to be recorded, a computer usable medium having computer readable program units embodied therein according to Claim 40, wherein the second program unit includes a program unit that reprograms each clock delay unit for the one data signal received in each sequence of n successive data signals.

43. In a precompensation circuit for magnetic recording of data signals having a clock generating clock signals at a predetermined rate in successive clock periods to clock the data signals to be recorded, a computer usable medium having computer readable program units embodied therein according to Claim 40, further comprising a third program unit for selecting output signals of the n clock delay units successively in each n data signal sequence to control the

recording times of the successive data signals of the sequence so that the clock delay data for the mth data signal is received by one of the n clock delay units while the output signal of the clock delay unit that is to receive the m+1th data signal controls the recording time of the (m-n+1)th data signal.

44. In a precompensation circuit for magnetic recording of data signals having a clock generating clock signals at a predetermined rate in successive clock periods to clock the data signals to be recorded, a computer usable medium having computer readable program units embodied therein according to Claim 40, wherein the first program unit includes:

a program unit for obtaining clock delay information from a look up table for each data signal responsive to the pattern of adjacent data signals;

a program unit for producing reference clock delay information corresponding to the predetermined clock rate; and

a program unit for combining the look up table clock data information for each data signal with the reference clock data information for the clock delay unit to which clock delay data for the data signal is sent to form the clock delay data for the data signal.

45. In a precompensation circuit for magnetic recording of data signals having a clock generating clock signals at a predetermined rate in successive clock periods to clock the data signals to be recorded, a computer usable medium

having computer readable program units embodied therein according to Claim 40, further comprising a fifth program unit responsive to a change in write clock rate for reprogramming the reference clock delay information of each clock delay unit responsive to a change in the predetermined clock rate.

46. A precompensation circuit for magnetic recording of data signals according to Claim 1, wherein said n > 1 clock delay units sequentially controls recording times of the successive data signals.

47. A precompensation circuit for magnetic recording of data signals according to Claim 27, wherein said n > 1 clock delay means sequentially controls recording times of the successive data signals.